KAS

Attorney Docket No. 039153-0256 (F0113)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yu

Title: A PROCESS FOR MANUFACTURING TRANSISTORS HAVING SILICON/GERMANIUM CHANNEL REGIONS

Appl. No.: 09/599,141

Filing Date: 06/22/2000

Examiner: Roman, A.

Art Unit: 2812

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on the date below.

Chris Escavalle
(Printed Name)

Chris Escavalle
(Signature)

8-1-02
(Date of Deposit)

DECLARATION UNDER 37 C.F.R. 1.131

Commissioner for Patents and Trademarks
Washington, D.C. 20231

Sir:

I, BIN YU, state and declare that:

1. I am the inventor of the invention recited in claims 1-24, 27, and 28 of the patent application identified above and an employee of Advanced Micro Devices, Inc., the Assignee of the patent application.

2. Prior to April 11, 2000, I conceived in the United States the subject matter of Claims 1-4, 11-24, 27, and 28 as evidenced by the attached Exhibit A.

3. Exhibit A (8 pages), titled " AMD INVENTION DISCLOSURE," marked "F0113," is a copy of an invention disclosure document used in the routine business practice of Advanced Micro Devices, Inc. for disclosing inventive subject matter to corporate patent counsel.

4. Exhibit A, received by AMD's Tech. Law Department on April 11, 2000, discloses the claimed subject matter of Claims 1-10, 12-24, 27, and 28. In particular, Figures (a)-(f) show an embodiment of each step of the process steps recited in claims 1-10, 12-24, 27, and 28.

5. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: 7/31/02

By: _____
Bin Yu

AMD

One AMD Place
P.O. Box 3453
Sunnyvale, CA 94088-3453
Tel (408) 732-2400

April 12, 2000

Joseph N. Ziebert
Foley, Lardner, Weissburg & Aronson
35th Floor
2029 Century Park East
Los Angeles, CA 90067

RE: Invention Disclosure F0113

Entitled: "SI/SIGE CHANNEL FORMED Y LASER THERMAL PROCESS"

Dear Mr. Ziebert:

Please prepare a US patent application for the subject invention disclosure and file the application in the USPTO within two months of this letter. A copy of the Invention Disclosure is enclosed.

Please follow the instructions set forth in AMD's DIRECTIONS TO OUTSIDE COUNSEL REGARDING PREPARATION AND PROSECUTION OF PATENT APPLICATIONS Version 1.0 dated May 1, 1996.

Also, please send us the formal drawings and the text in PCT format in accordance with AMD's directions provided to you.

If you have any questions or need additional information, please call me at 408-749-5177, or the responsible AMD Technology Law attorney, Dick Roddy at 408-749-2356.

Sincerely,

Shalini D'Shetty

Shalini Shetty
Patent Paralegal
Technology Law Department

Enclosure

/ala

cc:
Bin Yu

EXHIBIT A

COPY

AMD INVENTION DISCLOSURE

TLD ID# FF0113 rd

Rec'd date APR 11 2000

Sunnyvale x42110. return to MS 68. Texas x55964 return to MS 582

AMD TECH. LAW DEPT.

*********User see Readme*********

Project: ☐ **Product:** ☐ **Process:** ☒ **Technology** ☒ **to which the invention applies (*identify*):** Logic

List 2 to 5 key words useful to search by to find patents or art related to this invention: MOSFET, SiGe channel

Working title of invention: Si/SiGe Channel Formed By Laser Thermal Process

Inventor's signature :_____ **date** :2/24/00

Inventor's printed full name:Bin Yu Citizenship: China
Employee #: 24313 Extension: 42147 Mail stop: 143 Home telephone: 408-524-2780
Division: TRG Directorate: TRG Dept #: 7360 Department: STG Manager: M.R.Lin
Residence address: 1331 S. Wolfe Road, Sunnyvale, CA 94087
Post Office address: P.O.Box 3453, M/S 143, AMD, Sunnyvale, CA 94088

Co-Inventor's signature :_____ **date**:

Co Inventor's printed full name: Citizenship:
Employee #: Extension: Mail stop: Home telephone: - -
Division: Directorate: Dept #: 0 Department: Manager:
Residence address:
Post Office address:

Co-Inventor's signature :_____ **date**:

Co-Inventor's printed full name: Citizenship:
Employee #: Extension: Mail stop: Home telephone: - -
Division: Directorate: Dept #: Department: Manager:
Residence address:
Post Office address:

Co-Inventor's signature :_____ **date**:

Co-Inventor's printed full name: Citizenship:
Employee #: Extension: Mail stop: Home telephone: - -
Division: Directorate: Dept #: Department: Manager:
Residence address:
Post Office address:

List on additional sheet if there are more co-inventors and list total number of inventors here:

Name(s) of attorney(s) preferred by inventor(s) to prepare patent application, if known:

Attorney Joe Ziebert

Witness 1 initial: _____ Witness 2 initial: _____

Identify known relevant art ***(patents, publications, products)*****:**

State the problem solved by this invention: See attached sheets

Brief description and /or sketch of invention ***(attach copies of patent notebook pages, drawings or reports)***
See attached sheets

Patent notebook # 3 Page numbers: 70-72 Number of drawings: 6

AMD INVENTION DISCLOSURE

TLD ID#_____ Rec'd date _____

Sunnyvale x42110, return to MS 68. Texas x55964 return to MS 562

Advantages (check all that apply):

☐ avoids existing patent(s)	☒ improves precision	☐ simplifies manufacturing
☐ new function	☐ improves accuracy	☐ improves wear characteristic
☒ improves density	☒ improves efficiency	☐ improves signal to noise ratio
☒ increases operating speed	☐ fewer component parts	☐
☐ improves reliability	☐ reduces cost of manufacturing	☐

Discussion of advantage of the invention over other solutions
(***emphasize technical advance in the art as measured against known art***): See attached sheets

First written description* of invention, date: 2/24/00	First external disclosure to (name):
Date of first drawing*: 2/24/00 Date invention first reduced to practice:	Date of first external disclosure, none ☒ External disclosure under NDA* No ☐ Yes ☐
Made by (name): Bin Yu Tested by (name):	First external disclosure or use by: presentation ☐, announcement ☐, sample ☐, sale ☐, other ☐
Date of first computer simulation:	Date of Non-Disclosure Agreement*, if any:
Date of first successful test:	Date of first publication*:
Any of above occurred outside of USA ☐	Publication name:
* *attach copy if possible*	Date of first commercial use:

Does plan exist to publish, disclose or sell? If so, where and when?

Was invention conceived, constructed or tested pursuant to the performance under a development contract with another company: No ☒, Yes ☐. If yes, Company name:
If yes, name of AMD business contact and contract no.
Was invention jointly developed with participation of inventors from outside AMD. : No ☒ Yes ☐.
If yes, Company name:

I have read and understood this disclosure and read and signed each page of the attachments:

Witness 1 signature: Bin Yu Date: 4/6/2000
Printed name: Employee #: 24475

Witness 2 signature: Haiyan Wang Date: 4/7/2000
Printed name: Employee #: 25465

After completing to this point, deliver to department reviewer *date delivered*

Witness 1 initial: B. Y. Witness 2 initial: H.W.

AMD INVENTION DISCLOSURE

TLD ID# _____ Rec'd date _____
Sunnyvale x42110, return to MS 68, Texas x55964 return to MS 562

DISCLOSURE EVALUATION (*Entries from this point on are by the Reviewer*)

Does this invention add value to the AMD intellectual property portfolio? Yes ☐, No ☐ ☒ Maybe
Explain: This is highly inventive but also highly speculative whether or not the xtals will regrow with sufficient lack of defects is unknown. But SiGe is arousing interest + may be useful long term.

Do you know of any relevant art? Yes ☒, No ☐, **If yes, attach a copy and explain:**
Faintly related to the use of preamorphization and SPEG regrowth for highly doped Si regions. Also is not recrystallization of doped regions is known.

What application(s) do you foresee for this invention?
faintly possible alternate to MBE-type wfrs

I estimate the Value* of this invention disclosure is **A** ☐, **B** ☐, **C** ☒, **D** ☐,
* *use worksheet "Valuing Invention Disclosures and Patents"*
it **is** ☒, **is not** ☐ recommended to AMD for **U.S. patent application** filing,
it **is** ☐, **is not** ☒ recommended to AMD for **foreign patent application** filing,
it **is** ☐, **is not** ☐ recommended to be held as an **AMD trade secret**,
Give this high priority ☐, **normal** ☐, **low priority** ☒, **in patent application writing.**

GUIDELINES AND CONSIDERATIONS FOR FOREIGN FILING DECISION
Filing foreign patent applications is costly. We should choose to do it only when conditions warrant.
ALL CONDITIONS BELOW MUST APPLY IN ORDER TO INITIATE A FOREIGN FILING:

- ***Invention is High-Valued (A, B)*, and***
- ***Invention is in our technology path (usage), and***
- ***Invention usage is detectable by inspection of product, and***
- ***Invention is relatively hard to design around, and***
- ***Competitor is operating in the country of interest.*** *(see ca000000.xls tabulation of "Factory Sites outside the USA .)*

I recommend filing patent applications in foreign countries checked below:

Japan ☐	UK ☐	Taiwan ☐	S.Korea ☐	France ☐	Germany ☐
☐	☐	☐	☐	☐	☐

Reviewer's signature: _____ Employee #: 22264 Date: 10 April 2000
Reviewer's printed name: Matthews Buynoski

If foreign filing is checked, route to ***Div. VP*** for signature.

VP or Designate approves foreign filing (signature)_____

Reviewer: Complete this page and send (all) disclosures to TLD, including those not recommended for patent application filing.

Si/SiGe Channel Formed By Laser Thermal Process

Bin Yu
Strategic Technology Group

Background of This Disclosure

MOSFETs with SiGe channel have shown great advantages. Basically, the mobility of carrier (especially, holes) in SiGe could be 2-5 times larger than that in Si channel due to reduced carrier scattering and much lighter effective mass of holes in SiGe). The SiGe channel layer is usually very thin (a couple hundreds Angstroms) and the interface between Si substrate and SiGe layer needs to be very sharp. The conventional way to form SiGe channel is MBE (molacular beam epitaxy). However, MBE needs very complicated equipment that is not feasible for real production. In this disclosure, a new process method to form ultra-thin SiGe layer is proposed by using laser thermal process.

Highlights & Major Claims

The unique features of this new fabrication flow include (but not limited to):

(1) A very thin amorphous SiGe layer is deposited on top of the Si substrate. The a-SiGe layer is then recrystallized by laser thermal process.
(2) Because of the very short (a few nanoseconds) laser pulse, the thermal budget introduced is virtually negligible. Therefore the interface between Si substrate and SiGe channel layer is very sharp. There is no transition region.

Description of Process Flow

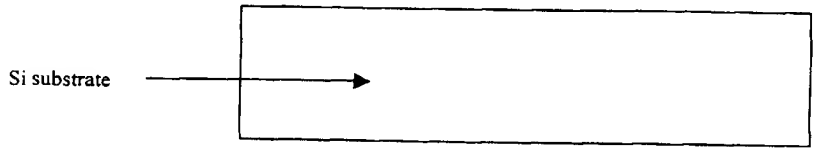
(a) Si substrate.
(b) LPCVD deposit a very thin (200-500A) amorphous SiGe layer.
(c) Exposed the wafer under excimer laser beam (e.g., 308nm wavelength). The melting temperature of a-SiGe (~1100∘C) is much lower than that of the single crystal Si (c-Si) substrate (~1400∘C). By controlling the laser fluence, the a-SiGe layer is fully melted without melting the c-Si substrate. A thin c-SiGe layer is formed by recrystallization after laser beam removed.
(d) LPCVD deposit a very thin (100-150A) a-Si layer.
(e) Exposed the wafer under excimer laser beam (e.g., 308nm wavelength). The melting temperature of a-Si (~1100∘C) is much lower than that of the c-SiGe/c-Si substrate. By controlling the laser fluence, the a-Si layer is fully melted without melting the c-SiGe/c-Si substrate. A thin c-Si layer is formed by recrystallization after laser beam removed. This thin c-Si layer is used as a cap layer above the SiGe channel layer to protect the gate oxide integrity.
(f) Regular CMOS fabrication flow to form transistor.

4/6/2000

4/7/2000

Drawing of Major Process Steps

(a)



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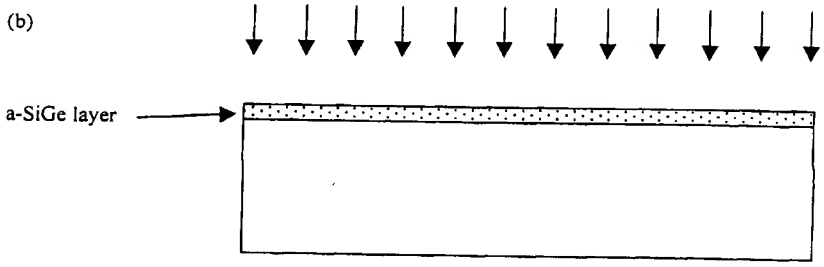
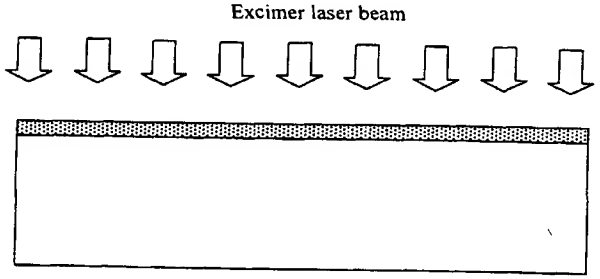


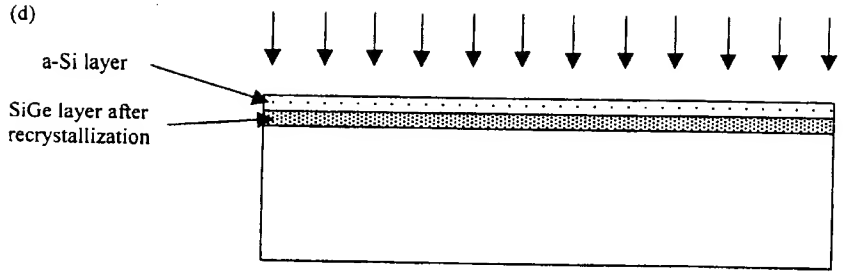
(c)



Qi Xi gu 4/6/2002

Haiyong Wang 4/7/2002

(d)



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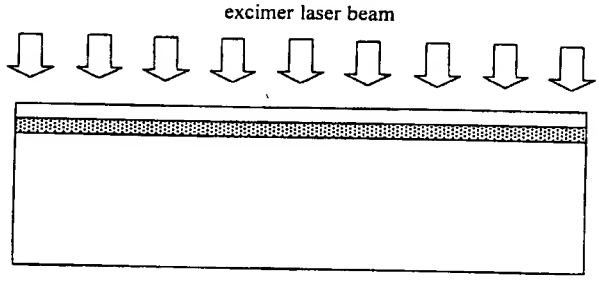
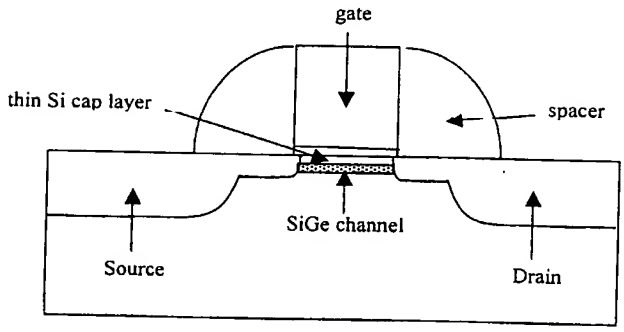


(t)



4/6/2000

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